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10/614,423	07/07/2003	Gireesh Shrimali	RAMB-01013US0	7449
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575 MARKET STREET SUITE 2500 SAN FRANCISCO, CA 94105			KANG, SUK JIN	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

			<u> </u>
	Application No.	Applicant(s)	
	10/614,423	SHRIMALI ET AL.	
Office Action Summary	Examiner	Art Unit	•
	Suk Jin Kang	2616	
The MAILING DATE of this communication a Period for Reply	ppears on the cover sheet v	vith the correspondence address	
A SHORTENED STATUTORY PERIOD FOR REP WHICHEVER IS LONGER, FROM THE MAILING - Extensions of time may be available under the provisions of 37 CFR after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory perions. - Failure to reply within the set or extended period for reply will, by stat Any reply received by the Office later than three months after the main earned patent term adjustment. See 37 CFR 1.704(b).	DATE OF THIS COMMUN 1.136(a). In no event, however, may a od will apply and will expire SIX (6) MO tute, cause the application to become A	ICATION. reply be timely filed NTHS from the mailing date of this communication. BANDONED (35 U.S.C. § 133).	
Status			
1) Responsive to communication(s) filed on 07	July 2003.		•
•—	nis action is non-final.		
3) Since this application is in condition for allow closed in accordance with the practice under	•	·	
Disposition of Claims		•	
4) ☑ Claim(s) 1-47 is/are pending in the application 4a) Of the above claim(s) is/are withdrest is/are allowed. 5) ☐ Claim(s) is/are allowed. 6) ☑ Claim(s) 1-47 is/are rejected. 7) ☐ Claim(s) is/are objected to. 8) ☐ Claim(s) are subject to restriction and	rawn from consideration.	·	
Application Papers			
9) The specification is objected to by the Exami 10) The drawing(s) filed on <u>03 December 2003</u> is Applicant may not request that any objection to the Replacement drawing sheet(s) including the correct of the oath or declaration is objected to by the	s/are: a)⊠ accepted or b)[ne drawing(s) be held in abeya ection is required if the drawin	nnce. See 37 CFR 1.85(a). g(s) is objected to. See 37 CFR 1.121(d).	
Priority under 35 U.S.C. § 119			
12) Acknowledgment is made of a claim for foreign a) All b) Some * c) None of: 1. Certified copies of the priority docume 2. Certified copies of the priority docume 3. Copies of the certified copies of the priority docume application from the International Bure * See the attached detailed Office action for a li	ents have been received. ents have been received in riority documents have bee eau (PCT Rule 17.2(a)).	Application No n received in this National Stage	
Attachment(s)	·		
1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)		Summary (PTO-413) (s)/Mail Date	

Paper No(s)/Mail Date 2/23/04.
U.S. Patent and Trademark Office
PTOL-326 (Rev. 08-06)

3) Information Disclosure Statement(s) (PTO/SB/08)

Paper No(s)/Mail Date. _ 5) Notice of Informal Patent Application

6) Other: _

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DETAILED ACTION

Priority

1. Applicant's claim for domestic priority under 35 U.S.C. 119(e) is acknowledged.

Information Disclosure Statement

2. The information disclosure statement submitted on February 23, 2004 has been considered by the Examiner and made of record in the application.

Claim Objections

- 3. Claims 4-9, 19, and 20 are objected to because of the following informalities:
 - a) On line 1 of claims 4-9, insert --of-- before "claim",
- b) On **line 3** of **claim 19** and **line 2** of **claim 20**, delete parentheses before and after "maximum negative value";

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Calamvokis (U.S. Patent # 6,735,212 B1).

Consider claim 1, Calamvokis discloses a method for scheduling multiple units of data requesting access to multiple ports in a network, the method comprising: generating a request matrix that represents requests from particular units of data for particular ports (column 5 lines 28-42, column 6 lines 5-14); generating a shuffle control that indicates a particular rearrangement of request matrix elements (column 6 lines 62-67, column 7 lines 1-8); generating a shuffled request matrix, including; rearranging, according the shuffle control, a set request matrix elements selected from a group comprising request matrix rows and request matrix columns (column 7 lines 33-41, column 8 lines 5-10); and rearranging, according to a reversed shuffle control, a set of matrix elements comprising a member of the group that was not selected to be rearranged according to the shuffle control (column 9 lines 30-42); performing arbitration on the shuffled request matrix to generate a shuffled grant matrix that represents shuffled granted requests (column 4 lines 61-67, column 6 lines 29-33); and generating a grant matrix, including applying a de-shuffle control to shuffled grant matrix elements including rows and columns (column 7 lines 61-63, column 13 lines 29-44).

Consider claim 2, and as applied to claim 1, Calamvokis discloses the method wherein the multiple units of data are cells (column 4 lines 61-67, column 6 lines 29-33) and the ports are egress ports of a packet switch (102, figure 2, column 4 lines 13-16), and wherein the method further comprises using the de-shuffled grant matrix to

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schedule a crossbar in the packet switch to perform cell transfers for one cell time (column 4 lines 12-21, column 6 lines 62-67, column 7 lines 1-2).

Consider claim 3, and as applied to claim 2, Calamvokis discloses the method wherein the rearranging according to the reversed shuffle control occurs at alternate cell times (column 13, lines 17-25).

Consider claim 4, and as applied to claim 3, Calamvokis discloses the method wherein at cell times during which the rearrangement according to the reversed shuffle control does not occur, the request matrix rows and columns are each rearranged according to the shuffle control (column 13, lines 17-25).

Consider claim 5, and as applied to claim 1, Calamvokis discloses the method wherein the shuffle control comprises a reassignment of positions among respective matrix elements, wherein the matrix elements include rows and columns (column 7 lines 36-63), and wherein the reversed shuffle control indicates a reassignment of positions among the respective matrix elements that is the reverse of the shuffle control reassignment (column 9 lines 30-42).

Consider claim 6, and as applied to claim 5, the method further comprising generating the shuffle control using software, including: performing a random_permute function to generate shuffle controls (column 7 lines 64-67, column 8 lines 1-10); storing the shuffle controls in a random access memory ("RAM") (column 5 lines 42-48); and accessing the generated shuffle controls in sequence to generate shuffled request matrices (column 5 lines 1-9 and 52-62).

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Consider claim 7, and as applied to claim 5, Calamvokis discloses the method further comprising generating the shuffle controls using at least one pseudo-random number generator (column 7 lines 1-29).

Consider claim 8, and as applied to claim 5, Calamvokis discloses the method further comprising deterministically generating the shuffle controls (abstract, column 2 lines 54-55, column 7 line 22-24).

Consider claim 9, and as applied to claim 1, Calamvokis discloses the method wherein the arbiter is a wrapped wavefront arbiter ("WWFA") (figure 7, column 5 lines 60-63, column 6 lines 44-60).

Consider claim 10. Calamyokis discloses a switch fabric, comprising: a plurality of ingress ports (102, figure 2, column 3 lines 51-52); a plurality of egress ports (102, figure 2, column 3 lines 51-52); a crossbar selectively configurable to couple ingress ports to egress ports (104, figure 2, column 4 lines 12-21); a scheduler coupled to the ingress ports, the egress ports, and the crossbar (106, figure 2), the scheduler comprising, a shuffle component (figure 8-9) that receives a shuffle control value that indicates a particular rearrangement of request matrix elements, wherein a request matrix represents requests from particular ingress ports for particular egress ports (column 5 lines 28-42, column 6 lines 5-14), and wherein the shuffle control component generates a shuffled request matrix (column 6 lines 62-67, column 7 lines 1-8), including, rearranging, according to the shuffle control value, a set of request matrix elements selected from a group comprising request matrix rows and request matrix columns (column 7 lines 33-41, column 8 lines 5-10); and rearranging, according to a

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reversed shuffle control value, a set of matrix elements comprising a member of the group that was not selected to be rearranged according to the shuffle control value (column 9 lines 30-42); performing arbitration on the shuffled request matrix to generate a shuffled grant matrix that represents shuffled granted requests (column 4 lines 61-67, column 6 lines 29-33); and a de-shuffle component that generates a grant matrix, including applying a de-shuffle control value to shuffled grant matrix elements including rows and columns (column 7 lines 61-63, column 13 lines 29-44); wherein the grant matrix is used to configure the crossbar (column 4 lines 12-21, column 5 lines 1-10).

Consider **claim 11**, and as applied to claim 10, Calamvokis discloses the switch fabric further comprising a shuffle/de-shuffle control component coupled to the shuffle component and to the de-shuffle component, wherein the shuffle/de-shuffle control component generates control signals under software direction from a central processing unit interface to configure the crossbar to perform data cell transfers from ingress ports to egress ports once each cell time (figure 1, figure 8-9, column 7 lines 38-41, column 8 lines 5-10).

Consider **claim 12**, and as applied to claim 10, Calamvokis discloses the switch fabric wherein the rearranging according to the reversed shuffle control value occurs at alternate cell times (column 13 lines 17-25).

Consider **claim 13**, and as applied to claim 12, Calamvokis discloses the switch fabric wherein at cell times during which the rearrangement according to the reversed shuffle control value does not occur, the request matrix rows and columns are each rearranged according to the shuffle control value (column 13 liens 17-25).

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Consider **claim 42**, Calamvokis discloses a method, comprising: generating a plurality of values, in the form of a matrix, representing a plurality of requests to transfer a plurality of data between a plurality of ingress ports and a plurality of egress ports (column 5 lines 28-42, column 6 lines 5-14); generating a random series of numbers representing matrix elements selected from a group comprising matrix rows and matrix columns; rearranging, responsive to the random series of numbers, a set of matrix elements selected from the group (column 6 lines 62-67, column 7 lines 1-8 and 33-41, column 8 lines 5-10); and, rearranging, responsive to a reverse random series of numbers, a set of matrix elements comprising a member of the group that was not selected to be rearranged responsive to the random series of numbers (column 9 lines 30-42).

Consider **claim 43**, and as applied to claim 42, Calamvokis discloses the method wherein the plurality of data are cells (column 4 lines 61-67, column 6 lines 29-33) and the plurality of egress ports are a plurality of egress ports of a packet switch (102, figure 2, column 4 lines 13-16).

Consider **claim 44**, and as applied to claim 42, Calamvokis discloses the method wherein the rearranging according to the reversed random series of numbers occurs at alternate cell times (column 13 lines 17-25).

6. Claims 14-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Ramamurthy et al. (U.S. Patent Application Publication # 2003/0227926 A1).

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Consider claim 14, Ramamurthy et al. discloses a method for scheduling data through a component in a network, the method comprising: allocating egress port bandwidth for each of a plurality of egress ports to various inputs (figure 1, [0028], [0029]); assigning credits to each of the various inputs in proportion to a predetermined bandwidth allocation for an egress port ([0049], [0050], [0093]); if an input requests access to an egress port and the input has at least one credit for the requested egress port, allowing the request to proceed to an arbiter ([0049], [0050], [0090]); and when an input receives a grant of access to a requested egress port from the arbiter, decrementing the credits of the input for the egress port by one ([0050]).

Consider claim 15, and as applied to claim 14, Ramamurthy et al. discloses the method further comprising: if an input has zero credits for an egress port, disallowing any requests from the input for the egress port from proceeding to the arbiter ([0090], [0109]); and when all of the inputs have zero credits for the egress port, resetting the credits, comprising reassigning credits to each of the various inputs in proportion to the predetermined bandwidth allocation for the egress port ([0050], [0110]).

Consider claim 16, and as applied to claim 14, Ramamurthy et al. discloses the method further comprising, when an input has a request for an egress port, the input has credits <= zero for the requested egress port, and no other inputs have pending requests for the egress port, allowing the request to proceed to the arbiter and decrementing the credits of the input for the egress port by one ([0050], [0126]).

Consider claim 17, and as applied to claim 16, Ramamurthy et al. discloses the method further comprising considering a priority assignment in allowing a request to

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proceed to an arbiter, including: assigning a first priority to requests from inputs that have credits >zero for the requested egress port ([0084], [0076]); and assigning a second priority to requests from inputs that have credits <= zero for the requested egress port, wherein second priority requests are only granted when no first priority requests are pending ([0084], [0076]).

Consider claim 18, and as applied to claim 16, Ramamurthy et al. discloses the method further comprising, when all of the inputs have credits <= zero for the egress port, updating the credits, comprising adding credits in proportion to the predetermined bandwidth allocation to each of the various inputs ([0093], [0107]).

Consider claim 19, and as applied to claim 16, Ramamurthy et al. discloses the method further comprising a maximum negative value, wherein the method further comprises, when an input has credits=(maximum negative value) for an egress port, disallowing any requests from the input for the egress port from proceeding to the arbiter ([0108], [0110]).

Consider claim 20, and as applied to claim 19, Ramamurthy et al. discloses the method further comprising, when all of the inputs have (maximum negative value) <= current credits <= zero for an egress port, updating the credits, comprising adding credits to the current credits for each of the various inputs in proportion to the bandwidth allocation for the egress port ([0093], [0107], [0138]).

Consider claim 21, and as applied to claim 14, Ramamurthy et al. discloses the method wherein the component comprises a packet switch (figure 1 and 4), and the various inputs comprise a plurality of ingress ports in the packet switch (figure 1, 4, and

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5b), and wherein each egress port of the packet switch individually allocates bandwidth among the ingress ports ([0018]).

Consider claim 22, and as applied to claim 14, Ramamurthy et al. discloses the method wherein the component comprises an input gueued with virtual output gueuing ("IQ with VOQ") packet switch with a plurality of ingress ports such that each ingress port of the component comprises a virtual output queue for each egress port, and wherein the various inputs comprise the virtual output queues (figure 4, [0042]).

Consider claim 23, and as applied to claim 14, Ramamurthy et al. discloses the method wherein the component comprises an input queued with virtual output queuing ("IQ with VOQ") packet switch with a plurality of ingress ports such that each ingress port of the component comprises a plurality of virtual output queues, and wherein each of the virtual output gueues corresponds to a combination of an egress port and at least one item selected from a group comprising a data class and a data priority (figure 4. [0042], [0049]).

Consider claim 24, Ramamurthy et al. discloses an apparatus for scheduling data through a network component, the apparatus comprising: a plurality of component ingress ports, each comprising a plurality of ingress port queues (figure 4); a plurality of ingress port processors, each receiving requests for access to multiple component egress ports from a plurality of ingress port queues (figure 5b, [0127]), wherein an egress port processor includes, credit update circuitry for receiving an initial number of credits for each queue, wherein the initial number of credits for a queue corresponds to an allocation of bandwidth by one egress port to one queue (figure 5b, [0029], [0107]);

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request processing circuitry coupled to the credit update circuitry and coupled to receive a request from a queue for access to an egress port, wherein the request processing circuitry determines whether to allow the request to proceed to an arbiter based on criteria including whether a requesting queue's number of credits is greater than a predetermined saturation value ([0049], [0076]-[0078]).

Consider **claim 25**, and as applied to claim 24, Ramamurthy et al. discloses the apparatus wherein the apparatus is cooperative with a strict priority scheme that assigns data one of a plurality of priorities, and wherein all data on the ingress ports is assigned a same priority for purposes of determining whether to allow a request to proceed to the arbiter ([0084]).

Consider **claim 26**, and as applied to claim 24, Ramamurthy et al. discloses the apparatus wherein the apparatus is cooperative with a strict priority assignment scheme that assigns data one of a plurality of priorities, and wherein all of the data on the ingress ports is initially assigned one priority for purposes of determining whether to allow a request to proceed to an arbiter ([0084]), and when a requesting queue's number of credits is equal to or less than zero, the requesting queue is assigned a different priority that is lower than the initially assigned priority, such that the requesting queue's request is allowed to proceed to the arbiter if no other queue with the initially assigned priority has a pending request for the egress port ([0050], [0090]).

Consider **claim 27**, and as applied to claim 24, the apparatus further comprising: grant allocation circuitry that receives a grant from the arbiter granting access to an egress port and allocates the grant to one of a plurality of data classes according to a

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predetermined allocation scheme (figure 6b, [0136], [0137]); request update circuitry coupled to the grant allocation circuitry for receiving the allocated grant and new requests (figure 6b, [0128], [0138], [0139]); and request count circuitry coupled to the request update circuitry for receiving the allocated grant and new requests and updating request counts for respective classes of data accordingly (figure 6b, [0138], [0139]).

Consider **claim 28**, and as applied to claim 27, Ramamurthy et al. discloses the apparatus wherein the credit update circuitry is further coupled to receive the allocated grant and, in response, decrement a number of credits for a queue that was allocated the grant ([0138], [0139]).

Consider **claim 29**, and as applied to claim 28, Ramamurthy et al. discloses the apparatus wherein: the request processing circuitry is coupled to the credit update circuitry to receive current credit values for all of the queues (figure 5b, [0092]); the request processing circuitry is coupled to the egress ports to send a flow_done signal to each egress port to indicate that all queues for a respective ingress port have exhausted their allocations of that egress port's bandwidth ([0092]); and the request processing circuitry receives an egress_done signal from each egress port indicating that the respective egress port has no pending requests from any ingress ports ([0092], [0126]).

Consider **claim 30**, and as applied to claim 29, Ramamurthy et al. discloses the apparatus wherein the credit update circuitry responds to the egress_done signal by resetting credits for each queue to the initial number ([0137], [0147]).

Consider **claim 45**, Ramamurthy et al. discloses a method, comprising: assigning a plurality of credit values to each of a respective plurality of inputs in proportion to a predetermined bandwidth allocation for an egress port (figure 1, [0049], [0050], [0093]); determining whether an input in the plurality of inputs requests access to the egress port ([0069], [0077]); determining whether a credit value associated with the input is greater than a predetermined threshold value ([0084], [0090], [0108]); allowing the request to proceed to an arbiter responsive to the determining steps ([0049], [0050], [0084]); and decrementing the credit value of the input for the egress port responsive to the input receiving a grant of access to the egress port from the arbiter ([0050], [0126]).

Consider **claim 46**, and as applied to claim 45, Ramamurthy et al. discloses the method wherein the threshold value is zero; and the method further comprises the step of: reassigning the plurality of credit values to each of the respective plurality of inputs in proportion to the predetermined bandwidth allocation for the egress port responsive to the plurality of credit values being zero ([0090], [0109], [0110]).

Consider **claim 47**, and as applied to claim 45, Ramamurthy et al. discloses the method wherein the allowing step further includes allowing the request to proceed when no other inputs have pending requests for the egress port ([0076], [0084]).

Claim Rejections - 35 USC § 103

- 7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

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the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the Examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the Examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

- 1. Determining the scope and contents of the prior art.
- 2. Ascertaining the differences between the prior art and the claims at issue.
- 3. Resolving the level of ordinary skill in the pertinent art.
- Considering objective evidence present in the application indicating obviousness or nonobviousness.
- 8. Claims 31-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ramamurthy et al. (U.S. Patent Application Publication # 2003/0227926 A1) in view of Calamvokis (U.S. Patent # 6,735,212 B1).

Consider **claim 31**, Ramamurthy et al. discloses a method for scheduling data through a network component in a network that uses a strict priority scheme, the method comprising: allocating egress port bandwidth for each of a plurality of

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component egress ports to various component ingress ports in a weighted round robin manner ([0167]), wherein the allocation includes assigning credits to each of the various ingress ports in proportion to a bandwidth allocation for an egress port ([0049], [0050], [0093]); determining which pending requests from ingress ports for egress ports will be passed to a crossbar scheduler, wherein the determination depends on a current number of credits assigned to an ingress port and a current strict priority assigned to the ingress port ([0049], [0050], [0076], [0090]); passing requests to the crossbar scheduler in the form of a request matrix ([0084]), but may not expressly disclose operating on the request matrix, including, generating a shuffled request matrix using the crossbar scheduler, including; rearranging, according to a shuffle control value, a set of request matrix elements selected from a group comprising request matrix rows and request matrix columns; and rearranging, according to a reversed shuffle control value, a set of matrix elements comprising a member of the group that was not selected to be rearranged according to the shuffle control value; performing arbitration on the shuffled request matrix using to generate a shuffled grant matrix that represents shuffled granted requests; generating a grant matrix, including applying a de-shuffle control value to shuffled grant matrix elements including rows and columns; and using the grant matrix to configure the crossbar.

In the same field of endeavor, Calamvokis discloses operating on the request matrix, including, generating a shuffled request matrix using the crossbar scheduler, including (column 5 lines 28-42, column 6 lines 5-14); rearranging, according to a shuffle control value, a set of request matrix elements selected from a group comprising

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request matrix rows and request matrix columns (column 6 lines 62-67, column 7 lines 1-8 and 33-41, column 8 lines 5-10); and rearranging, according to a reversed shuffle control value, a set of matrix elements comprising a member of the group that was not selected to be rearranged according to the shuffle control value (column 9 lines 30-42); performing arbitration on the shuffled request matrix using to generate a shuffled grant matrix that represents shuffled granted requests (column 4 lines 61-67, column 6 lines 29-33); generating a grant matrix, including applying a de-shuffle control value to shuffled grant matrix elements including rows and columns; and using the grant matrix to configure the crossbar (column 7 lines 61-63, column 13 lines 29-44).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the method of shuffling/de-shuffling matrices as taught by Calamvokis with the method of disclosed by Ramamurthy et al. for the purpose of effectively providing fairness, priority, and quality of service for scheduling.

Consider **claim 32**, and as applied to claim 31, Ramamurthy et al., as modified by Calamvokis, discloses the method wherein allocation occurs at at least two levels, including: a first level at which bandwidth is allocated among the ingress ports by a single egress port ([0028], [0029]); a second level at which bandwidth is allocated among multiple flows within each of the ingress ports, wherein a flow is characterized by an ingress port, an egress port, and a data class ([0034]); a third level at which bandwidth is allocated among items selected from a group comprising at least one subport and at least one data sub-class ([0028], [0070]).

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Consider **claim 33**, and as applied to claim 32, Ramamurthy et al., as modified by Calamvokis, discloses the method wherein multiple data classes are mapped to a single strict priority ([0028], [0084], [0085]).

Consider **claim 34**, and as applied to claim 31, Ramamurthy et al., as modified by Calamvokis, discloses the method wherein: all flows are initially assigned an initial number of credits in proportion to bandwidth allocated to the flow by an egress port ([0049], [0050], [0093]), and all flows are initially assigned a same strict priority ([0028], [0084], [0085]), and a flow's request for an egress port is passed to the scheduler when the flow has a credit balance for the egress port that is greater than zero ([0050], [0090]).

Consider **claim 35**, and as applied to claim 34, Ramamurthy et al., as modified by Calamvokis, discloses the method wherein all flows are reassigned the initial number of credits for an egress port when all flows have credit balances of zero for the egress port ([0050], [0110]).

Consider **claim 36**, and as applied to claim 31, Ramamurthy et al., as modified by Calamvokis, discloses the method wherein: all flows are initially assigned an initial number of credits in proportion to bandwidth allocated to the queue by an egress port ([0049], [0050], [0093]), and all flows are initially assigned a same strict priority; and if a flow has zero credits for the egress port, the flow is assigned a different strict priority that is lower than the initially assigned strict priority such that requests from the flow for the egress port may be passed to the scheduler if no flows with higher priority have pending requests for the egress port ([0076], [0084])

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Consider **claim 37**, and as applied to claim 36, Ramamurthy et al., as modified by Calamvokis, discloses the method further comprising a saturation number of credits, which is a negative number such that if a flow has the saturation number of credits for an egress port, no requests from the flow for the egress port will be passed to the crossbar scheduler ([0049], [0076], [0078]).

Consider **claim 38**, and as applied to claim 37, Ramamurthy et al., as modified by Calamvokis, discloses the method wherein, when all flows have the saturation credit number for an egress port, all flows are reassigned the initial numbers of credits and the initial same strict priority ([0028], [0084], [0085], [0110]).

Consider **claim 39**, and as applied to claim 31, Ramamurthy et al., as modified by Calamvokis, discloses the claimed invention, furthermore, Calamvokis discloses the method wherein the rearranging according to the reversed shuffle control occurs every other time the crossbar is configures (column 13 lines 17-25).

Consider **claim 40**, and as applied to claim 39, Ramamurthy et al., as modified by Calamvokis, discloses the claimed invention, furthermore, Calamvokis discloses the method wherein when the rearrangement according to the reversed shuffle control does not occur, the request matrix rows and columns are each rearranged according to the shuffle control value (column 13 lines 17-25).

Consider **claim 41**, and as applied to claim 40, Ramamurthy et al., as modified by Calamvokis, discloses the claimed invention, furthermore, Calamvokis discloses the method wherein when the shuffle control value indicates a reassignment of positions among respective matrix elements, wherein the matrix elements include rows and

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columns (column 7 lines 36-63), and wherein the reversed shuffle control value indicates a reassignment of positions among the respective matrix elements that is the reverse of the reassignment indicated by the shuffle control value (column 9 lines 30-42).

Conclusion

- The prior art made of record and not relied upon is considered pertinent to
 Applicant's disclosure.
 - a) Isoyama et al. (U.S. Patent Application Publication # 2001/0021191 A1)
 - b) Boduch et al. (U.S. Patent Application Publication # 2004/0085967 A1).
- 10. Any response to this Office Action should be **faxed to** (571) 273-8300 **or mailed to**:

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Hand-delivered responses should be brought to

Customer Service Window Randolph Building 401 Dulany Street Alexandria, VA 22314 Application/Control Number: 10/614,423 Page 20

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11. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Suk Jin Kang whose telephone number is (571) 270-

1771. The examiner can normally be reached on Monday - Friday 8:00-5:00 EST.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Chau Nguyen can be reached on (571) 272-3126. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or 703-305-3028.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist/customer service whose telephone number is (571) 272-2600.

Suk Jin Kang S.J.K./sik

June 22, 2007

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